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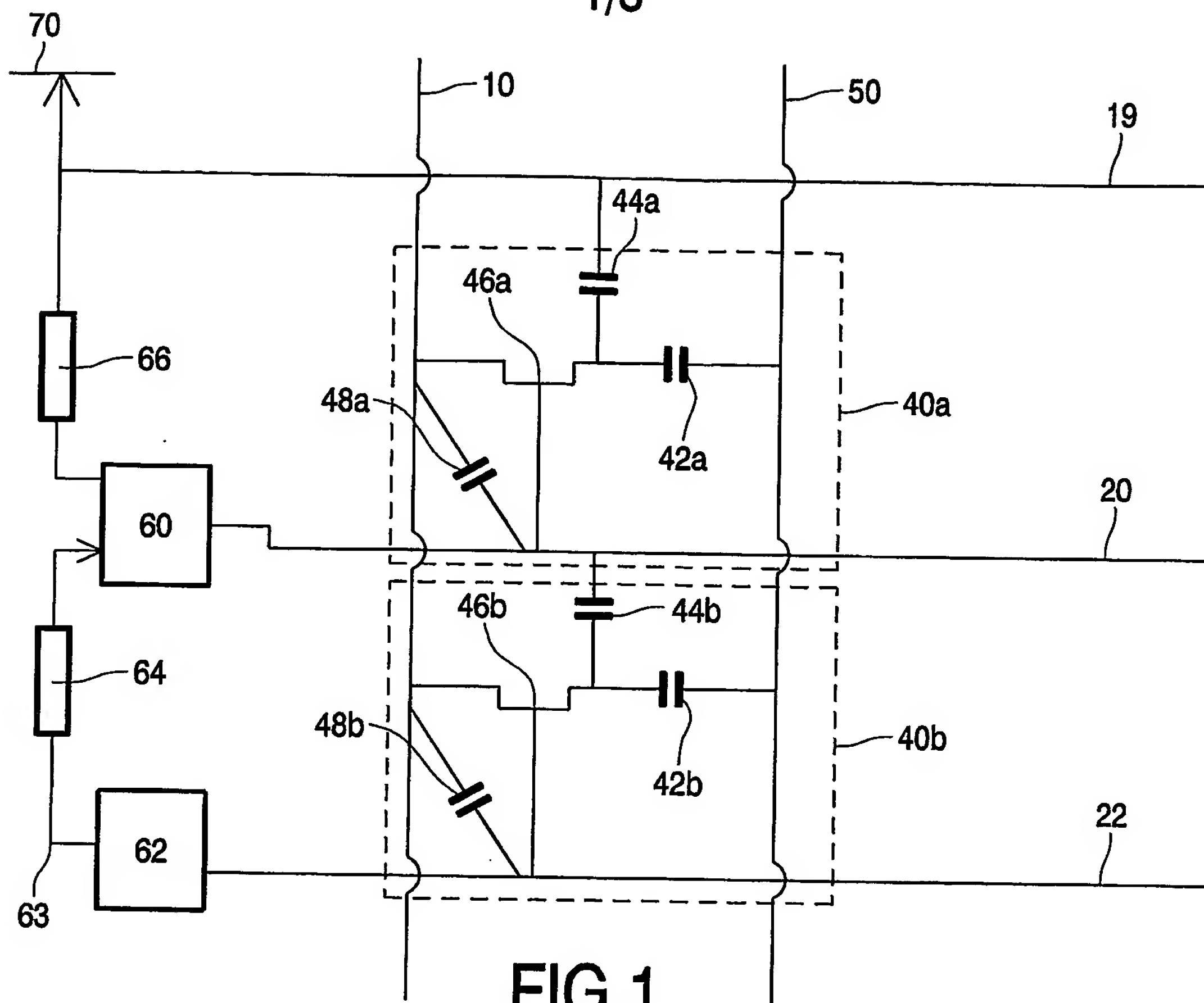


FIG. 1

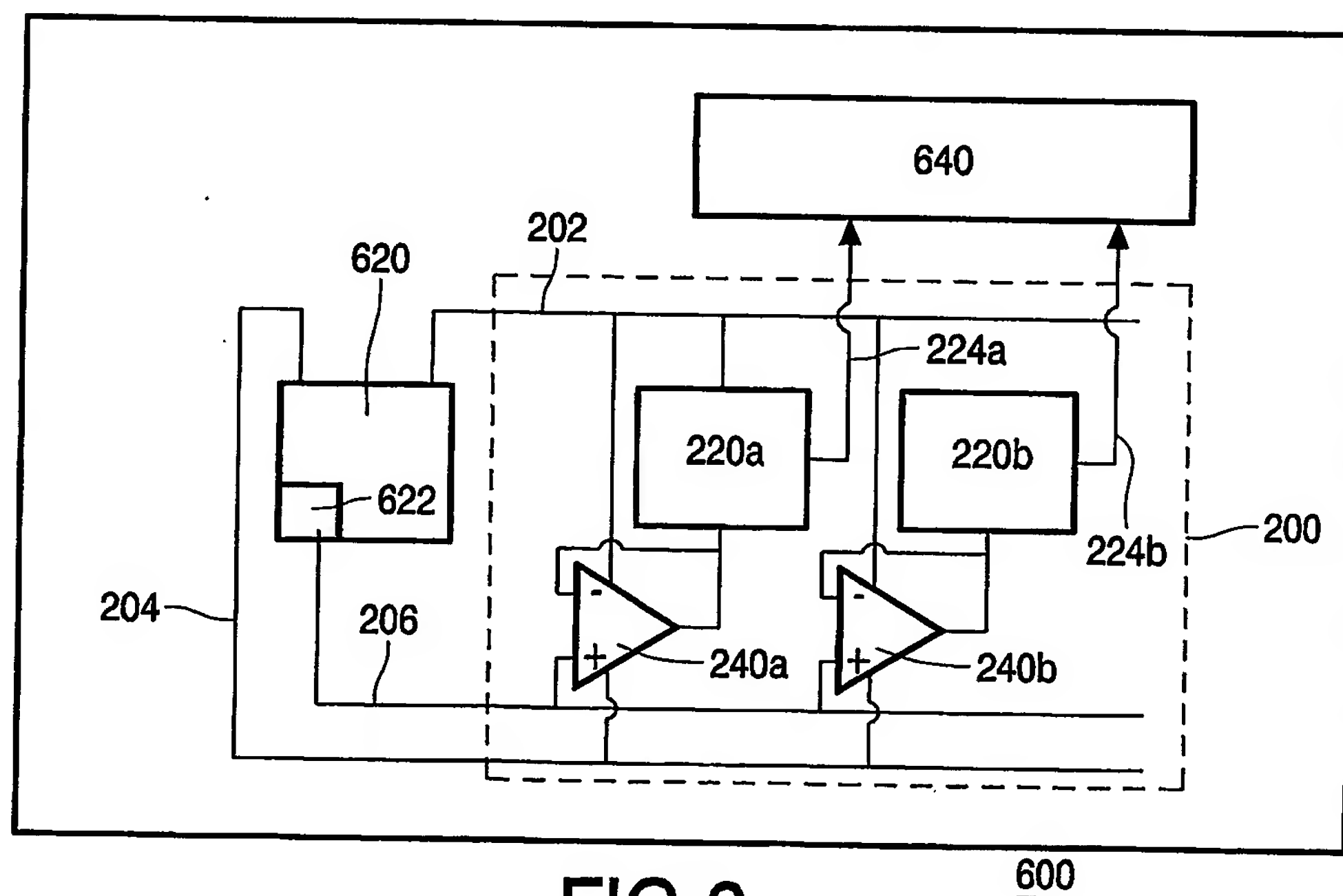
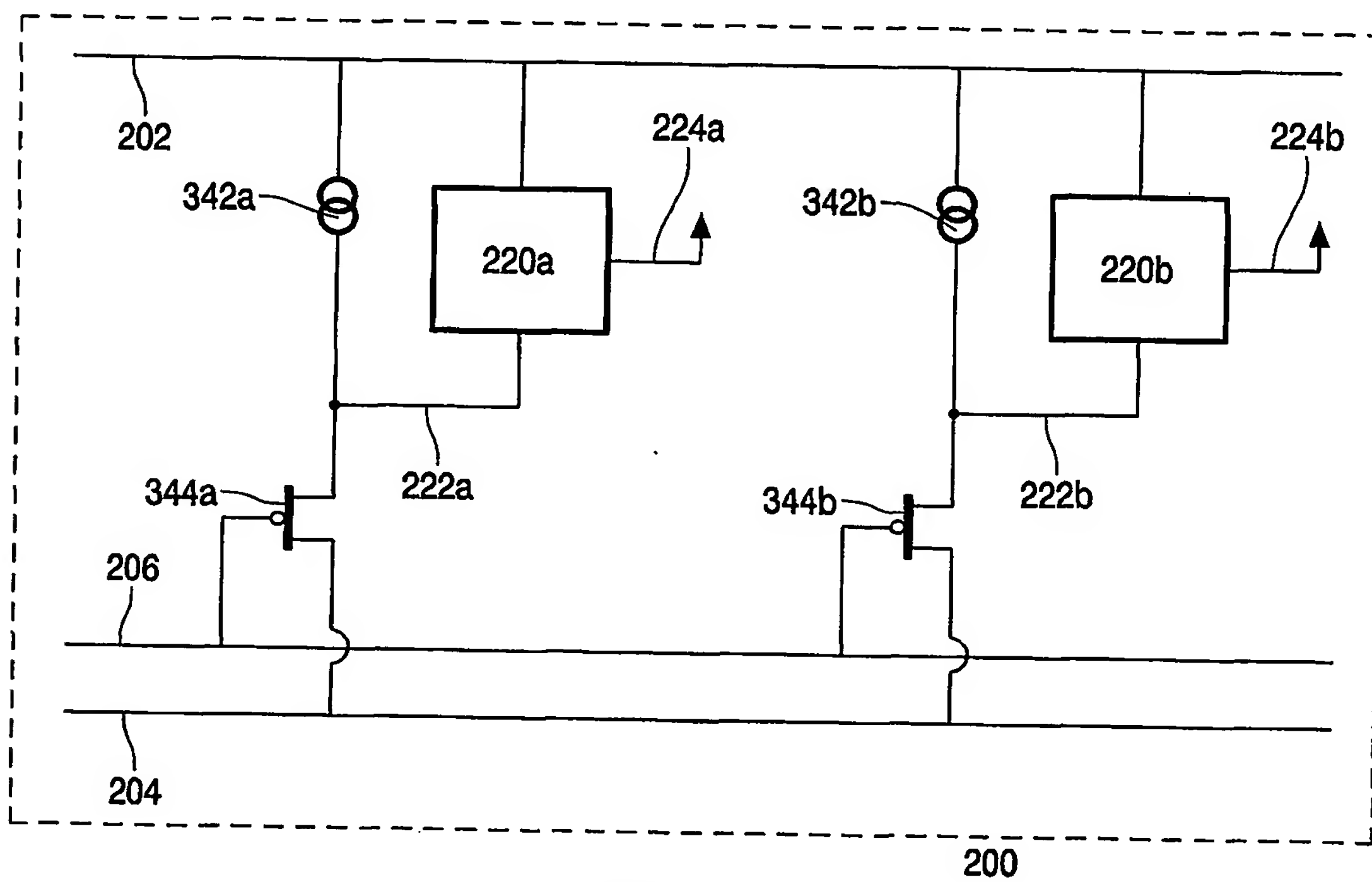


FIG. 6

The schematic diagram of circuit 200 shows a differential signal processing structure. It includes two input nodes, 202 and 206, which are connected to a pair of differential input transistors, 241a and 241b. The gates of these transistors are connected to a common gate signal 204. The sources of transistors 241a and 241b are connected to a common source node 208. The drains of transistors 241a and 241b are connected to a pair of differential load transistors, 220a and 220b. The gates of load transistors 220a and 220b are connected to a common gate signal 204. The sources of load transistors 220a and 220b are connected to a common source node 208. The drains of load transistors 220a and 220b are connected to a pair of differential output nodes, 224a and 224b. The gates of output transistors 220a and 220b are connected to a common gate signal 204. The sources of output transistors 220a and 220b are connected to a common source node 208. The drains of output transistors 220a and 220b are connected to a pair of differential output nodes, 224a and 224b. The gates of output transistors 220a and 220b are connected to a common gate signal 204. The sources of output transistors 220a and 220b are connected to a common source node 208. The drains of output transistors 220a and 220b are connected to a pair of differential output nodes, 224a and 224b.

200



200

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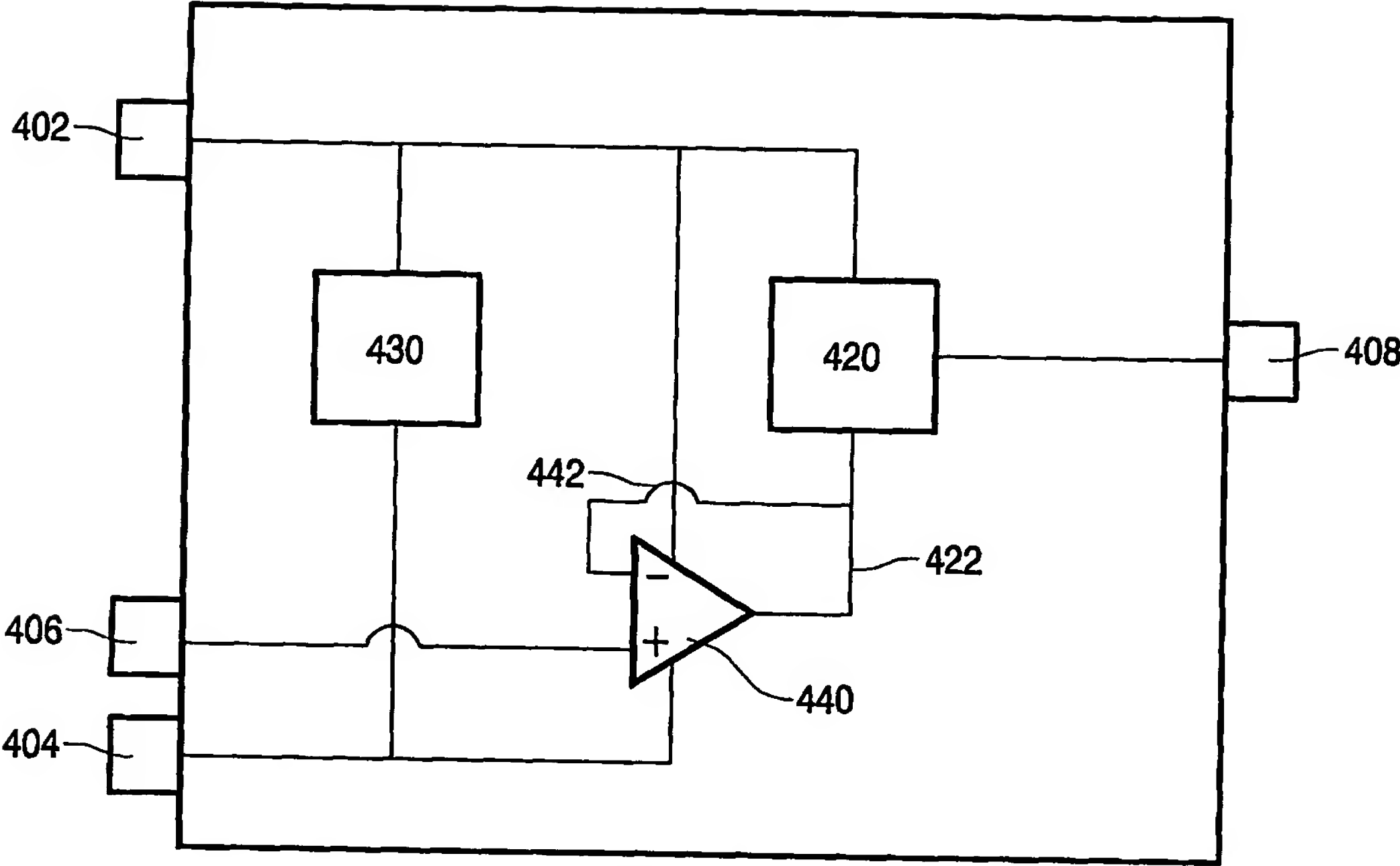


FIG.4 400

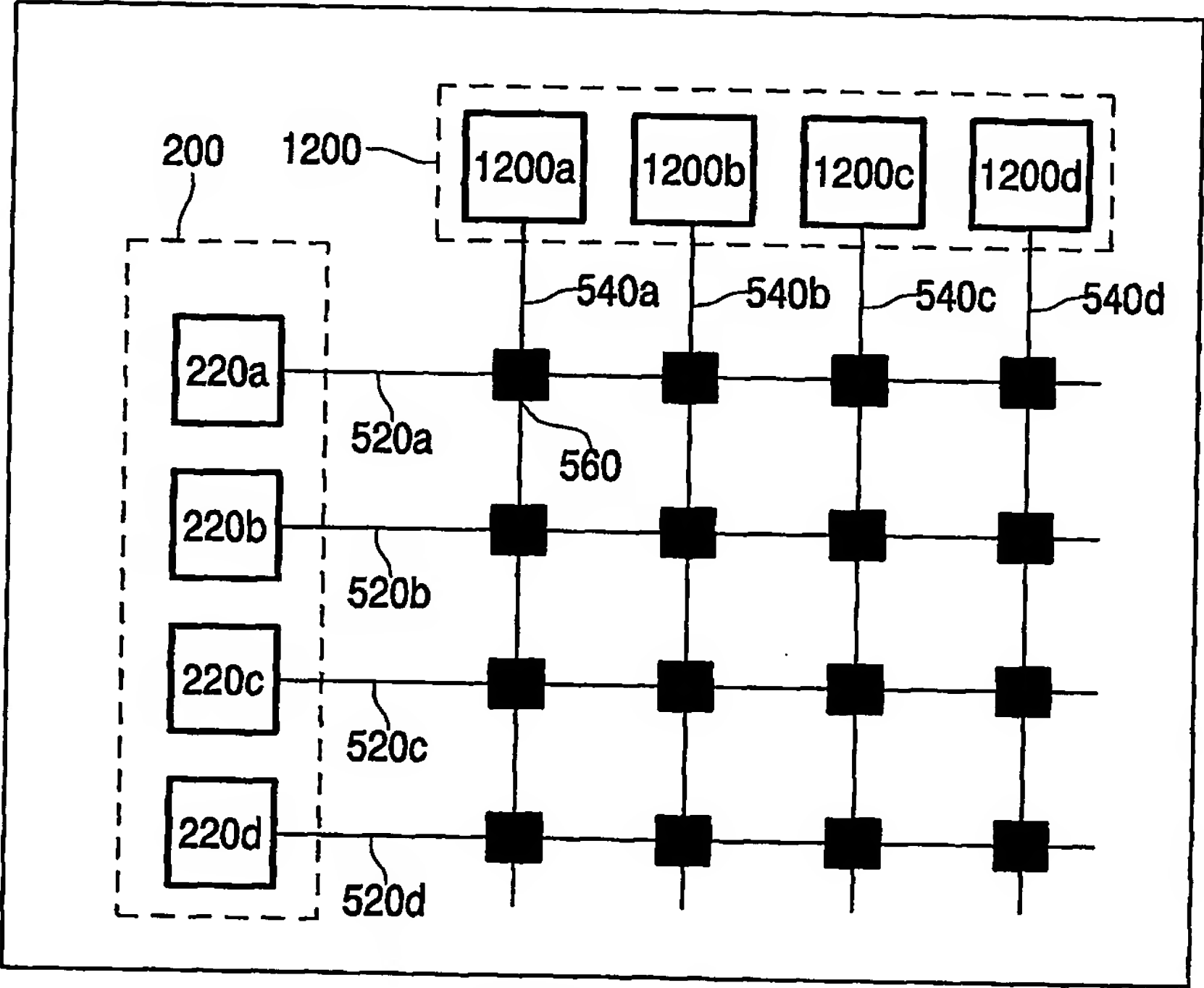


FIG.5 500